(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 107 302 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
13.06.2001 Bulletin 2001/24

(51) Int Cl.7: H01L 21/316

(21) Application number: 00126846.5

(22) Date of filing: 07.12.2000

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 07.12.1999 US 457086

(71) Applicant: Applied Materials, Inc.
Santa Clara, California 95054 (US)

(72) Inventors:
- Huang, Judy H.
Los Gatos, CA 95032 (US)
- Bencher, Christopher Dennis
Sunnyvale, CA 94087 (US)
- Rathi, Sudha
San Jose, CA 95132 (US)

(74) Representative:
Kirschner, Klaus Dieter, Dipl.-Phys.
Schneiders & Behrendt
Rechtsanwälte - Patentanwälte
Sollner Strasse 38
81479 München (DE)

(54) Method and apparatus for reducing fixed charges in a semiconductor device

(57) A method and apparatus for reducing trapped charges in a semiconductor device having a first layer and a second layer, said method comprising the steps of providing said first layer, flowing a deposition, a dilution and a conversion gas upon said first layer thereby forming a transition layer, phasing out said flow of conversion gas and forming said second layer upon said transition layer. The deposition gas, dilution gas and conversion gas are preferably trimethylsilane, helium and N_2O respectively. The method is performed via chemical vapor deposition or plasma enhanced chemical vapor deposition. The apparatus has a first insulating layer, a transition layer disposed upon said first layer and a second insulating layer disposed upon said transition layer. The transition layer improves the adhesion between said first insulating layer and said second insulating layer. A reduction in the amount of electrical charges (i.e., ions, electrons or the like) trapped between layers of deposited material improves the integrity and quality of devices formed from such layers.

EP 1 107 302 A2

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] The invention relates to the fabrication of semiconductor devices and, more particularly, the invention relates to a method and apparatus for reducing the amount of charges that are trapped between layers of a semiconductor device during its fabrication.

[0002] Integrated circuits fabricated on semiconductor substrates for Ultra Large Scale Integration (ULSI) require multiple levels of interconnections for electrically connecting the discrete semiconductor devices that comprise the circuits. Conventionally, the multiple levels of interconnections are separated by layers of insulating material. These interposed insulating layers have etched via holes which are used to connect one level of interconnections to another. Typically, the insulating layer material is silicon oxide (SiO_2) having a dielectric constant (relative to vacuum) of about 4.1 to 4.5. As device dimensions decrease and the device density increases, it is necessary to reduce the spacing between the interconnection levels to effectively connect the integrated circuits. Unfortunately, as the spacing decreases, the intra- (on the same metal level) and interlevel (between metal levels) capacitances increase when insulating layers therebetween have the same dielectric constant. The capacitance C is inversely proportional to the spacing d between the levels by the relationship C=keA/d where k is the dielectric coefficient, e is the permittivity of the insulator, A is the area, and d is the spacing between lines. Therefore, it is very desirable to minimize the dielectric constant k in the insulating layers between the interconnection layers to reduce the RC time constant and thereby increase the performance of the circuit (frequency response). The signal propagation time in the circuit is adversely affected by the RC delay time, where R is the resistance of the metal line, and C is the inter- and/or the intralevel capacitance mentioned above.

[0003] In greater detail, FIG. 1 depicts an integrated circuit device 100 that is presently known in the art. Typically the device 100 is comprised of a substrate material 102 (typically a dielectric material such as SiO_2) having a plurality of layers 103 of various materials disposed thereupon. The various layers have different electrical properties so as to create conductive pathways, circuit devices, and the like. For example, a first layer 104 is an insulating layer disposed on top of the substrate 102 acting as a primary insulator. Within the insulating layer 104 are various circuit pathways or circuit devices 106 comprised of conductive material such as titanium or aluminum. Disposed above the insulating and conductive layers, 104 and 106 respectively, is a second insulative layer 108. Typically, the second insulative layer 108 is a dielectric material but not necessarily the same material as the first dielectric layer 104.

[0004] One approach to minimize the RC time delays is to use a good electrical conductor for the interconnection levels, such as replacing the titanium or aluminum with copper to reduce resistance R. A second approach is to use an insulating material that has a lower dielectric constant k, such as an organic, to reduce the capacitance C between the interconnection levels. As such, it is highly favorable to use low k dielectric materials for the second insulative layer 108. One example of a typical low k dielectric material that is currently in use for the fabrication of integrated circuits is the compound trimethylsilane (3MS). The dielectric constant of this material is approximately 2.7; therefore, is highly preferred for use as a dielectric material between conductive areas such as conductive pathways and devices and the like represented as 106.

[0005] A well known method for creating integrated circuits such as those described above is by chemical vapor deposition (CVD). Typically, a precursor gas is mixed with a carrier gas and introduced to a deposition chamber at an elevated temperature. Upon contact with a substrate 102 within the chamber, the precursor gas decomposes into various elements and reacts with the surface to create the desired material (insulative layer 104, typically an oxide or conductive material 106, i.e., copper. Such processes may also be enhanced by the use of a plasma within the chamber which provides for a more uniform deposition process, i.e., when filling an opening in an oxide layer 104 with conductor material 106.

[0006] The second insulative layer 108 is also formed by CVD or plasma enhanced CVD; however, deficiencies in the process create undesirable results. For example when depositing one oxide material over another, i.e., second insulative layer 108 deposited over first insulative layer 104, different crystal planar structures and dimensions within these two materials create microscopic gaps at an interface 110 of two such layers. FIG. 2 shows an enlarged detail area of FIG. 1 depicting trapped electrical charges 202 at the interface 110 during the CVD process. These trapped charges 202 create a substantial charge buildup condition within the interface 110 which detrimentally effects nearby devices. For example FIG. 3 depicts a graph of capacitance vs. gate voltage of a device (i.e., the gate structure of a MOSFET transistor device) indicating a flat band voltage of approximately -55 V. Since the charge trapping condition is difficult to avoid, a typical and acceptable value for flat band voltage is approximately -15 V. If there are many such trapped charges 202 at the interface 110, devices constructed on the substrate are detrimentally effected resulting in poor or non-operational condition of such devices.

[0007] Therefore, there is a need in the art for a method of semiconductor IC construction and resultant apparatus having low k dielectric material to increase insulative properties, yet not creating the charge trap phenomenon at an interface between such low k dielectric material and other insulative materials used to construct such a device.

[0008] The disadvantages associated with the prior

art are overcome with the present invention of a method for reducing trapped charges in a semiconductor device having a first layer and a second layer, said method comprising the steps of providing said first layer, flowing a deposition, a dilution and a conversion gas upon said first layer thereby forming a transition layer, phasing out said flow of conversion gas and forming said second layer upon said transition layer. The deposition gas, dilution gas and conversion gas are preferably trimethylsilane, helium and N_2O respectively. Additionally, the step of phasing out the conversion gas flow alters the characteristics of the transition layer. The method is formed via chemical vapor deposition or plasma enhanced chemical vapor deposition when depositing the transition layer, first and second layers.

[0009] Alternately, a method for reducing trapped charges in a semiconductor device having a first layer and a second layer, said method comprising the steps of providing the first layer, flowing a deposition and dilution gas upon said first layer to form a transition layer thereupon, applying a plasma treatment to said transition layer, and forming said second layer upon said transition layer. The deposition gas and dilution gas are preferably trimethylsilane and helium respectively. Additionally, the plasma treatment further comprises a N_2O plasma conducted in a range of approximately 50 to 500 watts and preferably 250 watts. The second layer is preferably a trimethylsilane oxide layer.

[0010] An apparatus for reducing trapped charges in a semiconductor device is also disclosed. This apparatus has a first insulating layer, a transition layer disposed upon said first layer and a second insulating layer disposed upon said transition layer. The transition layer improves the adhesion between said first insulating layer and said second insulating layer and said transition layer is preferably a silicon carbide based material and most preferably SiC:H. The second insulating layer is trimethylsilane oxide.

[0011] With the method and apparatus described in the subject invention, a reduction in the amount of electrical charges (i.e., ions, electrons or the like) trapped between layers of deposited material is realized. As such, the integrity and quality of devices formed from such layers is improved.

[0012] The teachings of the present invention can be readily understood by considering the following detailed description of preferred embodiments in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a partial cross sectional view of a prior art semiconductor substrate having an integrated circuit constructed thereupon;

FIG. 2 depicts a detailed cross sectional view of the indicated area of FIG. 1;

FIG. 3 depicts a graph of capacitance vs. gate voltage measures at an interface of the integrated circuit of FIG. 1;

FIG. 4 depicts a partial cross sectional view of a semiconductor substrate having an integrated circuit constructed thereupon in accordance with the subject invention;

FIG. 5 depicts a graph of capacitance vs. gate voltage of the integrated circuit at an interface of the integrated circuit of FIG. 4 when using a method of the subject invention;

FIG. 6 depicts a graph of capacitance vs. a gate voltage of an integrated circuit of FIG. 4 when using an alternate embodiment of the method of the subject invention;

FIG. 7 depicts a series of method steps of the present invention;

FIG. 8 depicts a series of method steps of an alternate embodiment of the present invention; and

FIG. 9 depicts a deposition system used in conjunction with the the subject invention.

[0013] FIG. 4 depicts an integrated circuit device 400 in accordance with the present invention. The device 400 is comprised of a substrate material 402 (i.e., a dielectric material such as SiO_2) having a plurality of layers 403 of various materials disposed thereupon. The various layers have different electrical properties so as to create conductive pathways (also known as lines), circuit devices, and the like. These pathways and devices are linked to other devices on the substrate via a variety of other lines, interconnects and devices (not shown).

[0014] The device 400 is created by any known method and apparatus for fabricating integrated circuits and preferably by chemical vapor deposition (CVD). CVD and an apparatus for performing same is disclosed in US Patent No. 5,856,240 and is herein incorporated by reference. FIG. 9 depicts an exemplary deposition system 900 for performing CVD. A liquid precursor 918 is delivered to a deposition chamber 902 from a precursor delivery system 908 via one or more precursor material transfer lines 920. Specifically, the liquid precursor 918 is vaporized at vaporizer 906, mixed with a carrier gas 924 and delivered to a showerhead 922 in the deposition chamber 902. One example of a deposition chamber that can be used is a model DzX chamber manufactured by Applied Materials, Inc. of Santa Clara, California. The deposition chamber 902 contains a heated susceptor 916 for retaining the substrate 402 (i.e., a semiconductor wafer) onto which it is desirable to deposit the plurality of layers 403. Material is deposited onto the substrate 402 by CVD when the vaporized precursor contacts the heated substrate 402. Such processes may also be enhanced by the use of a plasma within the chamber which provides for a more uniform deposition process. The plasma is formed by driving one or more of the chamber components (i.e., the susceptor 916 or showerhead 922 with a high power energy source. For example, the energy source is an AC power source 928 connected to the susceptor 916. The chamber 902 and precursor delivery system 908 are controlled by a process control system 904.

[0015] The process chamber 902 is defined by a set of walls 914 that are electrically and thermally isolated from the susceptor 916 and showerhead 922 by isolators 910. Thermal energy, from a heating element 926 such as a resistive coil, heats a top surface of the susceptor 916. Pressure control unit 930 (i.e., a vacuum pump) adjusts the chamber atmosphere as necessary to facilitate deposition processes.

[0016] Returning to FIG. 4, a first layer 404 is an insulating layer disposed on top of the substrate 402 acting as a primary insulator. Within the insulating layer 404 are various circuit pathways or devices 406 comprised of conductive material such as titanium, copper, tantalum or the like. The first insulating layer 404 and conductive layer, disposed within a common plane, define an interface 410. A transition layer 407 is disposed upon the interface 410. Disposed above the transition layer 407, is a second insulative layer 408. Typically, the second insulative layer 408 is a dielectric material, but not necessarily the same material as the first dielectric layer 404.

[0017] The transition layer 407 is preferably a low k dielectric material. Such material has properties that enhance the bonding of the second insulative layer 408 to the first insulative layer 404. One such material that can accomplish this desired effect is BLOK™, a trademark of Applied Materials, Inc. of Santa Clara, CA. BLOK™ stands for Barrier LOw K dielectric material, is a silicon carbide based material and preferably has a K = 4.5.

[0018] The subject invention also includes a method for forming a second insulative layer upon a first insulative layer. Specifically, a first embodiment of the subject method is depicted in FIG. 7 as a series of method steps 700. The method begins at step 702 and proceeds to step 704 wherein a first insulative layer (i.e., an oxide layer) is provided on a substrate material. Said first insulative layer may be for example layer 404 disposed upon a semiconductor substrate 402 for defining conductive pathways or circuit devices upon said substrate. At step 706, a flow of deposition, dilution and conversion gases are provided to the first insulative layer. The deposition, dilution and conversion gases form a transition layer upon the first insulative layer. Said transition layer for example is layer 407 shown in FIG. 4. At step 708, the flow of conversion gas is phased out (i.e., gradually turned off or diminished over time). In phasing out the conversion gas, the characteristics of the transition layer are altered in a gradual fashion so as to improve the likelihood of adequate bonding between the transition layer and the second insulative layer. In step 710, a second insulative layer is formed upon the transition layer. The second oxide layer is, for example, layer 408 as shown in FIG. 4.

[0019] In the above discussed method 700, the deposition gas is a silicon based material and in a preferred embodiment of the invention is trimethylsilane (3MS), the dilution gas is an inert gas and in a preferred embodiment is helium. The conversion gas is an oxygen containing gas and in a preferred embodiment of the invention is N_2O. Additionally, the second insulative layer is a silicon based insulating layer and in a preferred embodiment of the invention is a trimethylsilane oxide layer.

[0020] The above discussed first insulative, transition, and second insulative layers are created via methods to those skilled in the art of semiconductor circuit device fabrication and include but are not limited to physical vapor deposition (PVD), chemical vapor deposition (CVD) and the like and in a preferred embodiment of the invention the subject layers are formed via CVD, and more preferably by plasma enhanced CVD (PECVD). The subject method can be practiced in a semiconductor fabrication chamber such as a DxZ chamber a manufactured and sold by Applied Materials, Inc. of Santa Clara, CA. The conditions under which such method takes place are as follows:

T = 350°C - 400°C, preferably 350C
Pressure 2 - 20 Torr, preferably 8.7 Torr
Power 50 - 500 Watts, preferably 250 Watts
Electrode spacing 350-600 mils, preferably 435 mils
Conversion gas flow 500-2500 sccm, preferably 1500 seem N_2O
3MS flow 25-500 sccm
He flow 100-2000 seem

[0021] In an alternate embodiment of the invention depicted in FIG. 8, a series of method steps 800 is used to form a second insulative layer upon a first insulative layer. Such method steps 800 begin at step 802 and proceed to step 804 wherein a first insulative layer is provided on a substrate. At step 806, a flow of deposition and dilution gases is provided upon a first insulative layer to form a transition layer thereupon. In step 808, the flow of deposition and dilution gases is halted and a plasma treatment is applied to the transition layer. The plasma treatment alters the characteristics of the transition layer so as to improve the adhesion of the second insulative layer. At step 810, the second insulative layer is disposed upon the transition layer and the method 800 concludes at step 812.

[0022] The benefits of the above-discussed apparatus are seen by comparing FIGS. 5 and 6 to FIG. 3. FIG. 5 depicts a graph of gate voltage (V) vs. capacitance (pF) for a semiconductor device formed in accordance with either of the methods disclosed. Specifically, the flatband voltage has been reduced to approximately -25V as compared to -55V of the untreated (i.e., no transition layer) device , the flatband voltage of which device is shown in FIG. 3. FIG. 6 depicts a graph of the same characteristic for a device that has been treated under more optimized conditions (including the use of Silane) as disclosed above. In this device, the flatband voltage has been reduced to the typically acceptable value of -15V. A flatband voltage closer zero indicates that there are fewer charges trapped in the interface 410 of the

subject invention than previously realized. As such, the device 400 is less susceptible to breakdown caused by generally poor or out-of-spec design.

Claims

1. Method for reducing trapped charges in a semiconductor device having a first layer and a second layer, said method comprising the steps of:

   providing said first layer;
   flowing a deposition, a dilution and a conversion gas upon said first layer thereby forming a transition layer;
   phasing out said flow of conversion gas; and
   forming said second layer upon said transition layer.

2. The method of claim 1 wherein said conversion gas is N_2O.

3. The method of claim 1 wherein the step of phasing out the conversion gas flow is designed to alter the characteristics of the transition layer.

4. Method for reducing trapped charges in a semiconductor device having a first layer and a second layer, said method comprising the steps of:

   providing the first layer;
   flowing a deposition and dilution gas upon said first layer to form a transition layer thereupon;
   applying a plasma treatment to said transition layer; and
   forming said second layer upon said transition layer.

5. The method of any of the preceding claims wherein said deposition gas is trimethylsilane.

6. The method of any of the preceding claims wherein said dilution gas is helium.

7. The method of claim 4 wherein said plasma treatment further comprises a N_2O plasma.

8. The method of claim 7 wherein said plasma treatment is conducted in a range of approximately 50 to 500 watts, preferably at 250 watts.

9. The method of any of the preceding claims wherein said transition layer, said first and said second layer are formed via chemical vapor deposition or via plasma enhanced chemical vapor deposition.

10. The method of any of the preceding claims wherein said first layer and said second layer are insulating layers.

11. The method of claim 10 wherein said second layer is a trimethylsilane oxide layer.

12. An apparatus for reducing trapped charges in a semiconductor device comprising:

    a first insulating layer;
    a transition layer disposed upon said first layer; and
    a second insulating layer disposed upon said transition layer.

13. The apparatus of claim 12 wherein said transition layer is designed to improve the adhesion between said first insulating layer and said second insulating layer.

14. The apparatus of claim 12 wherein said transition layer further comprises a silicon carbide based material, preferably SiC:H.

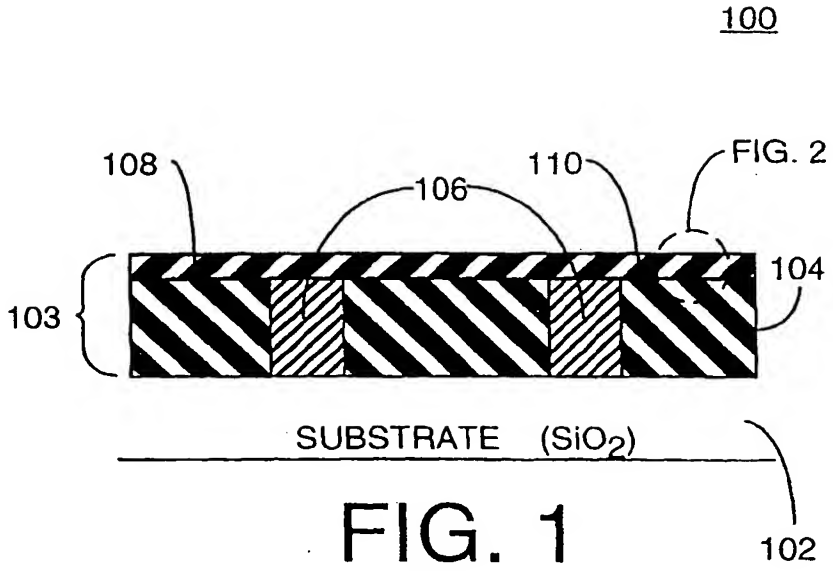

FIG. 1
PRIOR ART

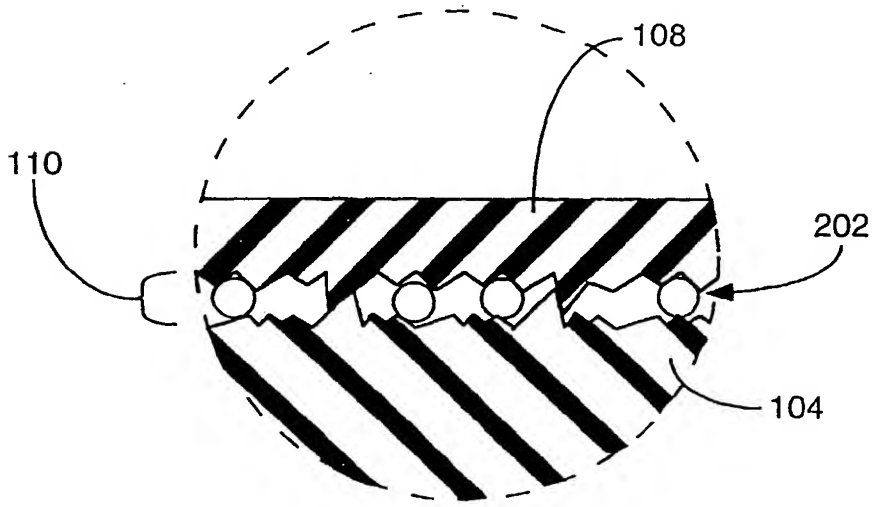

FIG. 2
PRIOR ART

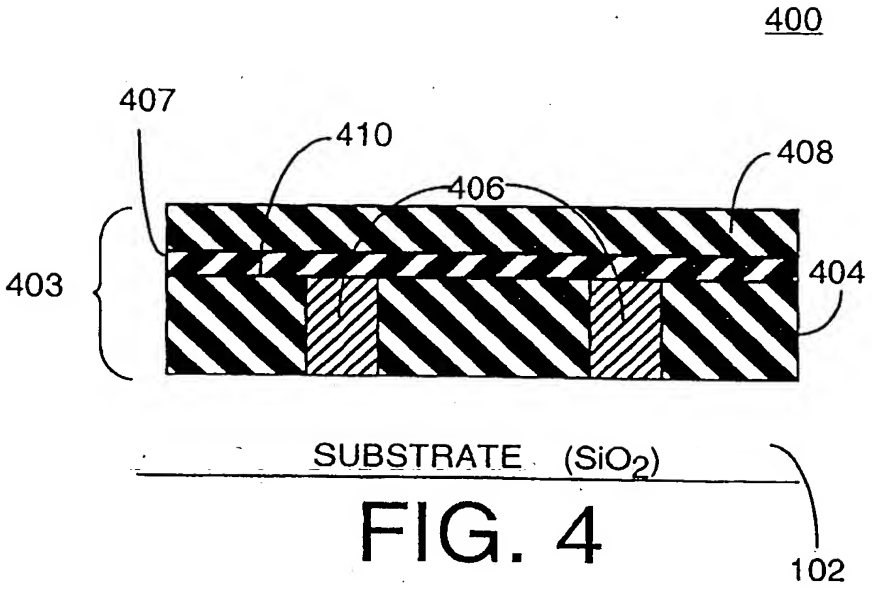

FIG. 4

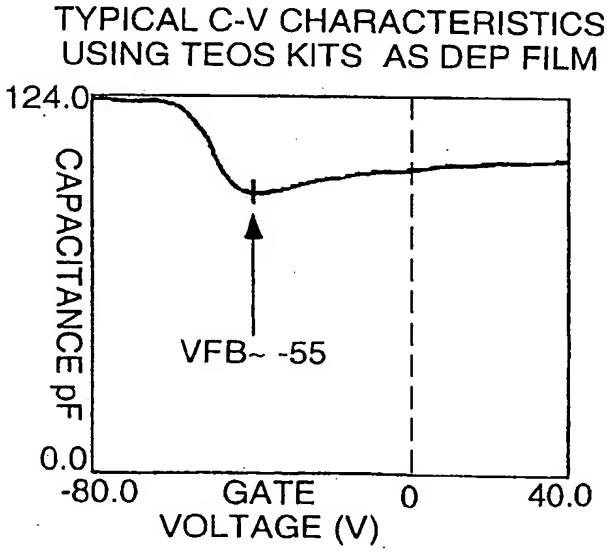

FIG. 3
PRIOR ART

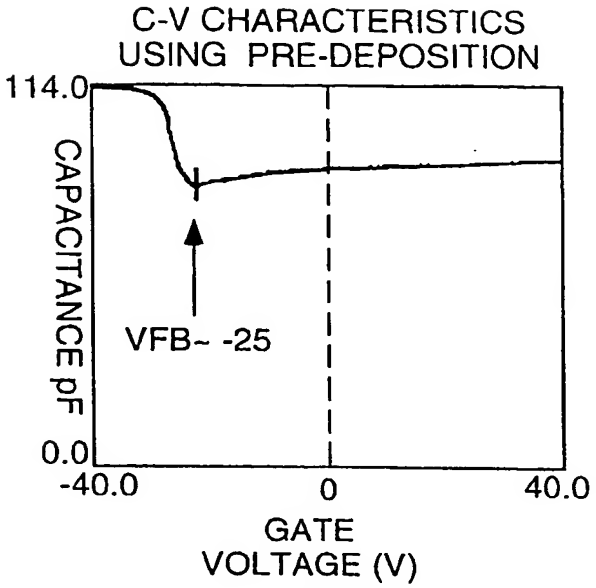

FIG. 5

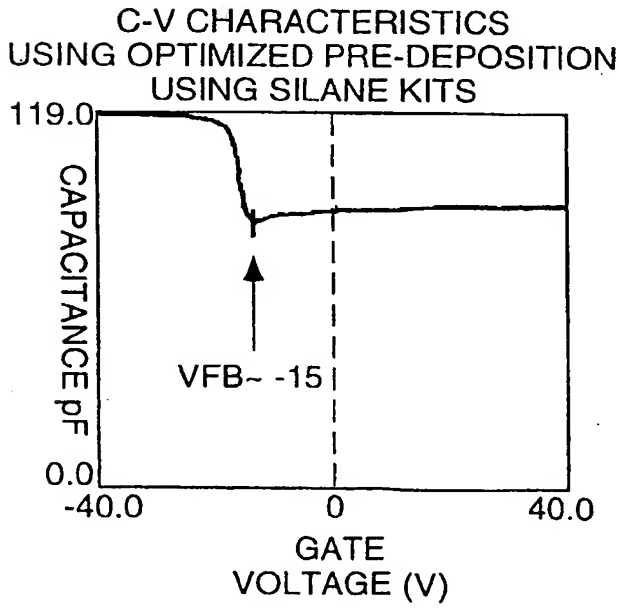

FIG. 6

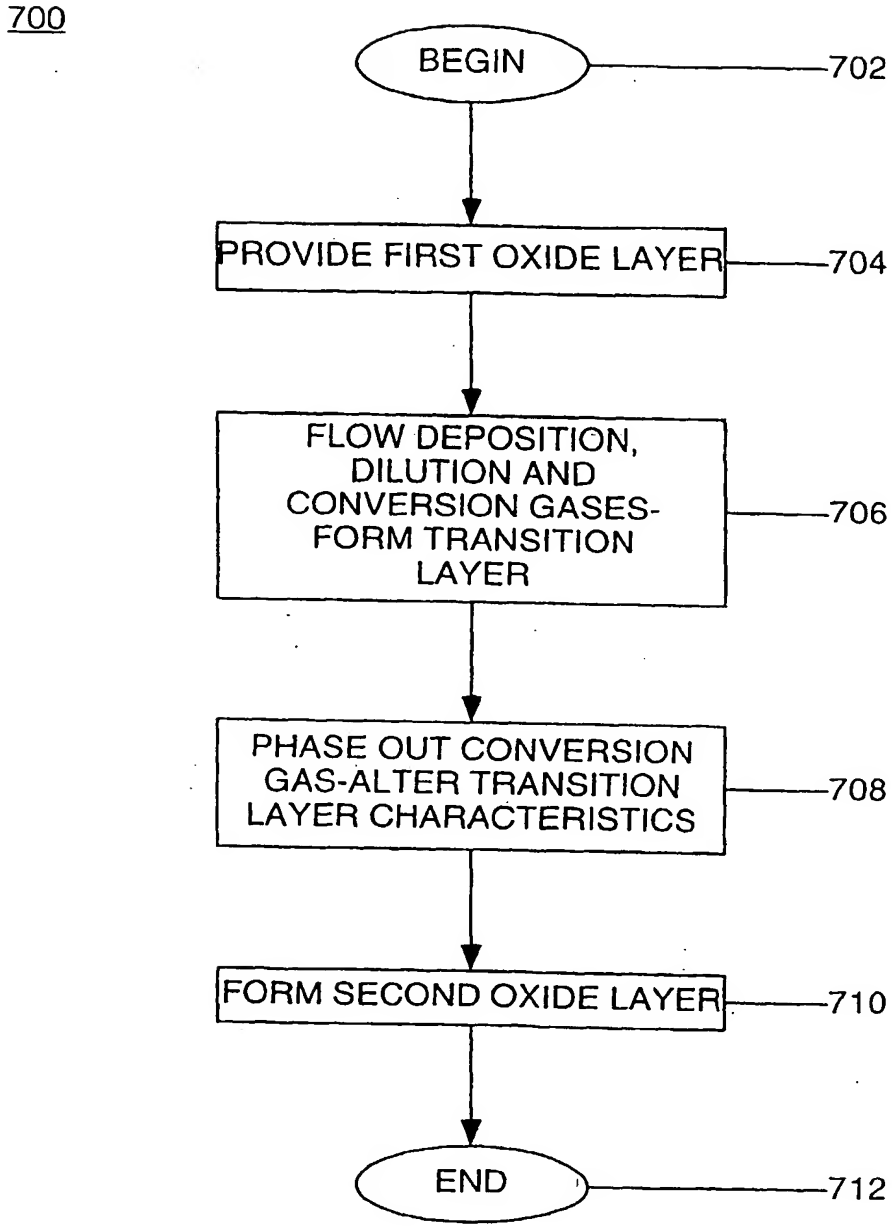

FIG. 7

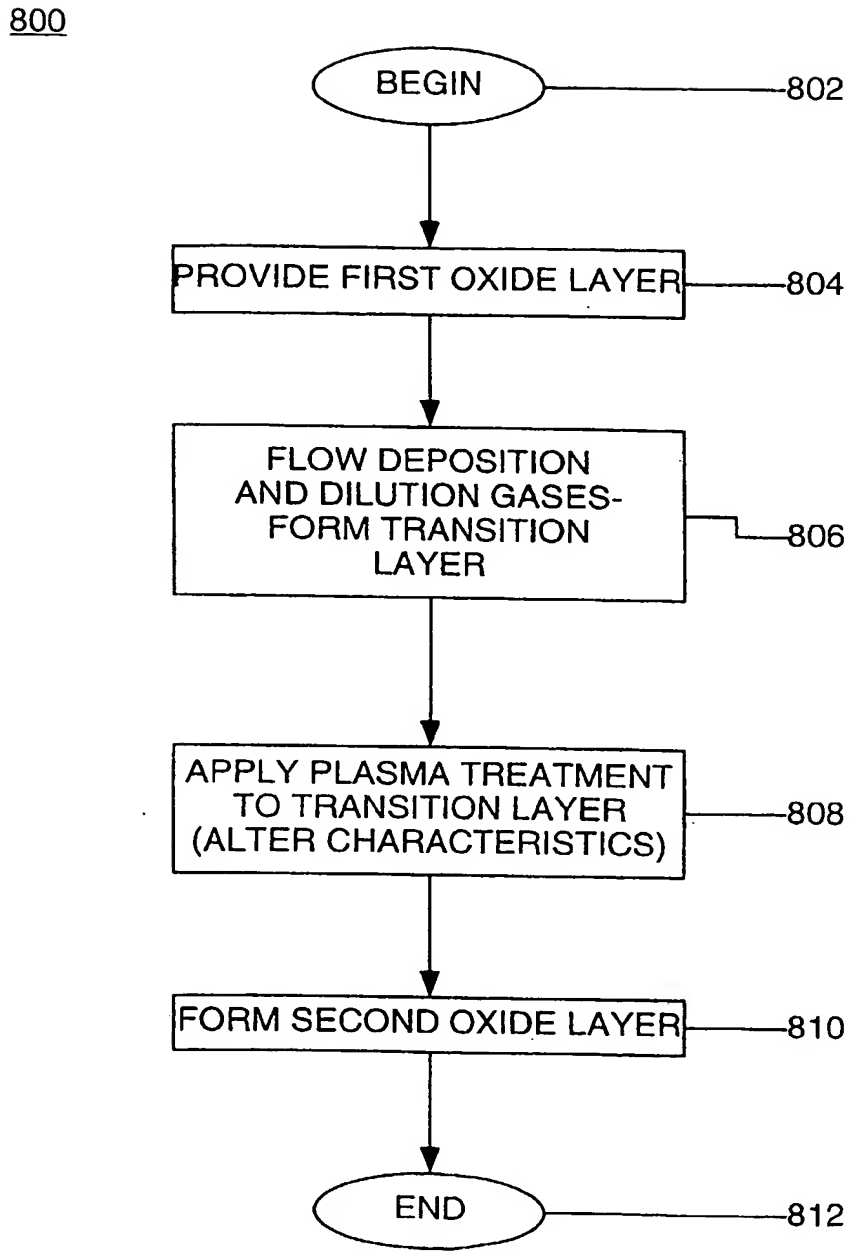

FIG. 8

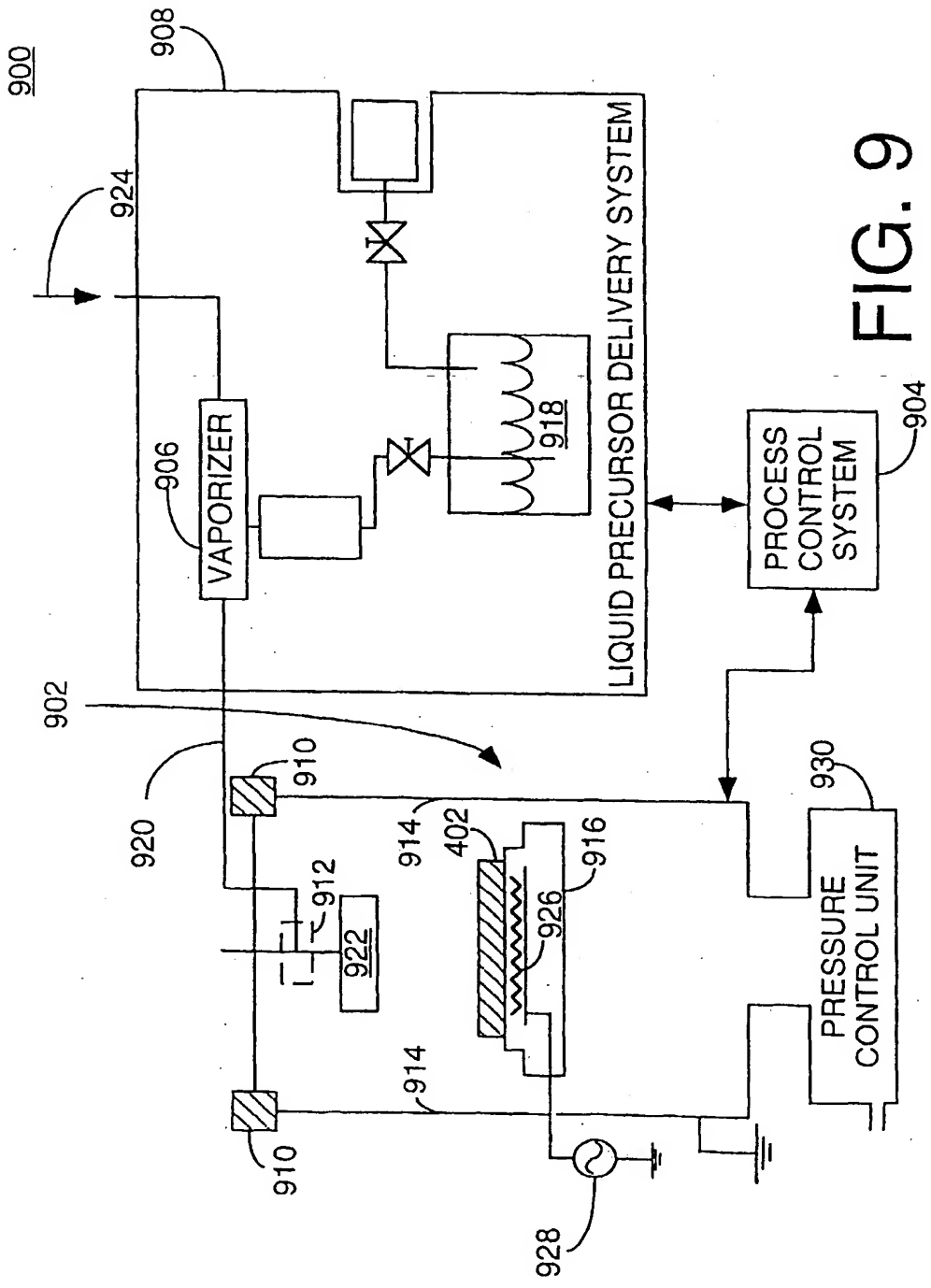

FIG. 9

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 107 302 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
27.10.2004 Bulletin 2004/44

(43) Date of publication A2:
13.06.2001 Bulletin 2001/24

(51) Int Cl.[7]: **H01L 21/316**

(21) Application number: **00126846.5**

(22) Date of filing: **07.12.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **07.12.1999 US 457086**

(71) Applicant: **Applied Materials, Inc.**
Santa Clara, California 95054 (US)

(72) Inventors:
- **Huang, Judy H.**
  Los Gatos, CA 95032 (US)
- **Bencher, Christopher Dennis**
  Sunnyvale, CA 94087 (US)
- **Rathi, Sudha**
  San Jose, CA 95132 (US)

(74) Representative:
Kirschner, Klaus Dieter, Dipl.-Phys.
Böck, Tappe, Kirschner
Rechtsanwälte - Patentanwälte
Sollner Strasse 38
81479 München (DE)

(54) Method and apparatus for reducing fixed charges in a semiconductor device

(57) A method and apparatus for reducing trapped charges in a semiconductor device having a first layer and a second layer, said method comprising the steps of providing said first layer, flowing a deposition, a dilution and a conversion gas upon said first layer thereby forming a transition layer, phasing out said flow of conversion gas and forming said second layer upon said transition layer. The deposition gas, dilution gas and conversion gas are preferably trimethylsilane, helium and N_2O respectively. The method is performed via chemical vapor deposition or plasma enhanced chemical vapor deposition. The apparatus has a first insulating layer, a transition layer disposed upon said first layer and a second insulating layer disposed upon said transition layer. The transition layer improves the adhesion between said first insulating layer and said second insulating layer. A reduction in the amount of electrical charges (i.e., ions, electrons or the like) trapped between layers of deposited material improves the integrity and quality of devices formed from such layers.

EP 1 107 302 A3

Printed by Jouve, 75001 PARIS (FR)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 12 6846

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X Y	US 5 965 203 A (GABRIC ZVONIMIR ET AL) 12 October 1999 (1999-10-12) * the whole document *	1,3,6,9, 10,12 2,5,11, 13,14	H01L21/316
Y	EP 0 960 958 A (DOW CORNING) 1 December 1999 (1999-12-01) * the whole document *	2,5,11	
Y	WO 99/41423 A (APPLIED MATERIALS INC) 19 August 1999 (1999-08-19) * page 4, line 1 - page 26, line 8; figures 10A,10B *	13,14	
A	US 5 943 599 A (TSAI KWONG-JR ET AL) 24 August 1999 (1999-08-24) * abstract *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L
C23C

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
The Hague	2 June 2004	Bakker, J

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ISDOCID: <EP_____1107302A3_I_>

European Patent Office

Application Number
EP 00 12 6846

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1-3, 5, 6, 9-14

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 00 12 6846

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-3, 5, 6, 9-14

Method of depositing a semiconductor device comprising the step of depositing a graded transition layer and corresponding device.

---

2. claims: 4-14

Method of forming a semiconductor device comprising the steps of depositing a homogeneous layer and plasma treatment and corresponding device.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 12 6846

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

02-06-2004

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5965203 A	12-10-1999	DE 19516669 A1	07-11-1996
		AT 182926 T	15-08-1999
		DE 59602585 D1	09-09-1999
		EP 0741196 A1	06-11-1996
		JP 3502504 B2	02-03-2004
		JP 8306685 A	22-11-1996
		TW 424116 B	01-03-2001
EP 0960958 A	01-12-1999	US 6159871 A	12-12-2000
		EP 0960958 A2	01-12-1999
		JP 2000049157 A	18-02-2000
		SG 72955 A1	23-05-2000
		TW 491910 B	21-06-2002
		US 6593655 B1	15-07-2003
		US 2003111662 A1	19-06-2003
WO 9941423 A	19-08-1999	US 6054379 A	25-04-2000
		US 6072227 A	06-06-2000
		US 6287990 B1	11-09-2001
		US 2001004479 A1	21-06-2001
		EP 1055012 A2	29-11-2000
		JP 2002503879 T	05-02-2002
		TW 408369 B	11-10-2000
		US 2002074309 A1	20-06-2002
		US 2002084257 A1	04-07-2002
		WO 9941423 A2	19-08-1999
		US 2003064610 A1	03-04-2003
		US 2001005546 A1	28-06-2001
		US 2003113992 A1	19-06-2003
		US 6340435 B1	22-01-2002
		US 6413583 B1	02-07-2002
		US 6511909 B1	28-01-2003
		US 2003162410 A1	28-08-2003
		US 6511903 B1	28-01-2003
		US 2002000670 A1	03-01-2002
		US 6593247 B1	15-07-2003
		US 6660663 B1	09-12-2003
		US 6537929 B1	25-03-2003
		US 6562690 B1	13-05-2003
		US 6541282 B1	01-04-2003
		US 2004029400 A1	12-02-2004
		US 2004082199 A1	29-04-2004
		US 2004038545 A1	26-02-2004
		US 6627532 B1	30-09-2003
		US 2004147109 A1	29-07-2004
		US 2004166665 A1	26-08-2004

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 12 6846

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

02-06-2004

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9941423 A		US 2002045361 A1	18-04-2002
		US 6596655 B1	22-07-2003
		US 2002111042 A1	15-08-2002
		US 2003124859 A1	03-07-2003
US 5943599 A	24-08-1999	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82